In the Claims:

1. (Original) A nonvolatile memory device having a write mode of operation, comprising:

a write/read controller configured to selectively control write/read control signals enabled in the write mode;

a nonvolatile resistive memory device coupled to receive write/read control signals from the write/read controller; and

a logic switch having two or more switching states configured to select among the switching states depending on a logic value stored in the nonvolatile resistive memory device when the write/read control signals are disabled.

2. (Original) The nonvolatile memory device according to claim 1, wherein the write/read controller comprises:

a first NMOS transistor controlled by a first write control signal;

a first PMOS transistor connected in parallel to the first NMOS transistor and controlled by a second write control signal having an opposite phase to the first write control signal.

3. (Original) The nonvolatile memory device according to claim 1, wherein the nonvolatile resistive memory device comprises:

a first resistive memory device having a resistive state connected between a first input node and an output node of the write/read controller; and

a second resistive memory device having a settable resistive state connected between a second input node and the output node of the write/read controller.

4. (Original) The nonvolatile memory device according to claim 3, wherein the selection of a switching state of the logic switch is determined based on a state of a first input signal inputted into the first resistive memory device when the first resistive memory device is set at a low resistance state and the second resistive memory device is set at a high resistance

state, and

the selection of a switching state of the logic switch is determined based on a state of a second input signal inputted into the second resistive memory device when the first resistive memory device is set at a high resistance state and the second resistive memory device is set at a low resistance state.

5. (Original) The nonvolatile memory device according to claim 4, wherein each of the first and the second resistive memory devices comprises:

a first electrode connected to one of the first input node or the second input node;

a second electrode connected to an output node of the write/read controller; and

a phase change layer formed between the first electrode and the second electrode.

6. (Original) The nonvolatile memory device according to claim 1, wherein the nonvolatile resistive memory device comprises at least one of a phase change memory device, a magnetoresistive device and a metal memory device.

7. (Original) A nonvolatile memory device, comprising:

a flip-flop unit comprising a PMOS latch configured to latch a datum and a NMOS latch configured to latch a complement of the datum;

a nonvolatile resistive memory device connected between the PMOS latch and the NMOS latch;

an access controller for controlling a connection of a bitline and the flip-flop unit depending on an enable state of a wordline; and

a current supply unit configured to supply current for changing data stored in the nonvolatile resistive memory device when write/read control signals are enabled.

8. (Original) The nonvolatile memory device according to claim 7, wherein gate input signals of the PMOS latch and the NMOS latch are connected to the nonvolatile resistive

memory device with either a positive feedback type circuit or a negative feedback type circuit.

9. (Original) The nonvolatile memory device according to claim 7, wherein the nonvolatile resistive memory device comprises a first resistive memory device and a second resistive memory device, each of the first and second resistive memory devices configured to store different logic values depending on a difference in an amount of current generated by a voltage applied to the bitline when the write/read control signals are enabled.

10. (Original) The nonvolatile memory device according to claim 9, wherein each of the first resistive memory device and the second resistive memory device comprises:

a first electrode connected to the PMOS latch;

a second electrode connected to the NMOS latch; and

a phase change layer formed between the first electrode and the second electrode.

11. (Original) The device according to claim 7, wherein the current supply unit comprises a first PMOS transistor and a second PMOS transistor, each of the first and second PMOS transistors configured to be connected in parallel to the PMOS latch and to have a gate configured to receive the write/read control signals.

12. (Original) A nonvolatile memory device, comprising:

a flip-flop unit comprising a NMOS latch for latching data;

a nonvolatile resistive memory device, connected between a power voltage terminal and the flip-flop unit; and

an access controller for controlling a connection of a bitline and the flip-flop unit depending on an enable state of a wordline.

13. (Original) The nonvolatile memory device according to claim 12, wherein the NMOS latch comprises a first NMOS transistor and a second NMOS transistor configured to be

connected between the resistive memory device and a ground voltage terminal with a latch type circuit, and

gate input signals of the first and the second NMOS transistors are connected to the nonvolatile resistive memory device with either a positive feedback type circuit or a negative feedback type circuit.

14. (Original) The nonvolatile memory device according to claim 12, wherein the nonvolatile resistive memory device comprises a first resistive memory device and a second resistive memory device, each of the first and second resistive memory device configured to store different logic values depending on a difference in an amount of current generated by a voltage applied to the bitline.

15. (Original) The nonvolatile memory device according to claim 14, wherein each of the first and the second resistive memory devices comprises:

a first electrode connected to the power voltage terminal;

a second electrode connected to the NMOS latch; and

a phase change layer formed between the first electrode and the second electrode.

16. (Original) The nonvolatile memory device according to claim 12, further comprising a driver circuit configured to supply a power voltage to the nonvolatile resistive memory device when write/read control signals are enabled.

17. (Currently Amended) A nonvolatile memory device, comprising:

a flip-flop unit including a NMOS latch for latching a datum and its complement;

an access controller for controlling a connection of a bitline to the flip-flop unit depending on an enable state of a wordline; and

~~a nonvolatile resistive~~ a phase change memory device connected between the flip-flop unit and the access controller.

18. (Currently Amended) The nonvolatile memory device according to claim 17, wherein the NMOS latch comprises a first NMOS transistor and a second NMOS transistor configured to be connected between the ~~resistive~~ phase change memory device and a ground voltage terminal with a latch circuit, and

gate input signals of the first and the second NMOS transistors are connected to the ~~nonvolatile resistive~~ phase change memory device with a positive feedback type circuit.

19. (Currently Amended) The nonvolatile memory device according to claim 17, wherein the ~~nonvolatile resistive~~ phase change memory device comprises a first ~~resistive~~ phase change memory device and a second ~~resistive~~ phase change memory device, each ~~resistive~~ phase change memory device configured to store different logic values depending on a difference in an amount of current generated by a voltage applied to the bitline.

20. (Currently Amended) The nonvolatile memory device according to claim 19, wherein each of the first and the second ~~resistive~~ phase change memory device comprises:

a first electrode connected to the access controller;

a second electrode connected to the NMOS latch; and

a phase change layer formed between the first electrode and the second electrode.

21. (Original) An electronic device, comprising:

a write/read controller means for selectively controlling write/read control signals enabled in a write mode;

a resistive memory means for storing data based on states of resistance that can be changed by passing an amount of current through the means when the write/read control signals are enabled; and

a logic switch means for selecting among switching states based on logic values stored in the resistive memory means when the write/read control signals are disabled.

22. (Currently Amended) An electronic device comprising:

a means for latching data;

a ~~resistive~~ phase change memory means for storing data as states of resistance that can be set by an applied electrical current, the ~~resistive~~ phase change memory means being coupled to the means for latching data;

an access controller means for connecting a data input to the means for latching data in response to an enable state of a wordline; and

a current supply means for supplying current to the ~~resistive~~ phase change memory means for changing a resistive state in response to a write control signal.

23. (Original) A method for storing data in a memory, comprising the steps of:

selectively controlling write/read control signals enabled in a write mode of a controller;

storing data in a resistive memory based on states of resistance that can be changed by passing an amount of current through the resistive memory when the write/read control signals are enabled; and

selecting among switching states based on logic values stored in the resistive memory when the write/read control signals are disabled.